Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/TE0712+CPLD

1 Overview

Firmware for PCB CPLD with designator U3: LCMX02-256HC

1.1 Feature Summary

- JTAG Multiplexer
- Module Power sequencing
- FPGA Configuration sequencing
- LED Status and User access
- FPGA IO User access

1.2 Firmware Revision and supported PCB Revision

See Document Change History

2 Product Specification

2.1 Port Description

Name / opt. VHD Name	Direction	Pin	Description
JTAGEN	in	26	Switch JTAG between CPLD and FPGA (logical one for CPLD, logical zero for FPGA)
TMS / M_TMS	IN	29	JTAG from B2B connector
TCK / M_TCK	IN	30	JTAG from B2B connector
TDI / M_TDI	IN	32	JTAG from B2B connector
TDO / M_TDO	OUT	1	JTAG from B2B connector

Name / opt. VHD Name	Direction	Pin	Description
F_TMS / C_TMS	OUT	21	JTAG to FPGA
F_TCK / C_TCK	OUT	17	JTAG to FPGA
F_TDI / C_TDI	OUT	23	JTAG to FPGA
F_TDO / C_TDO	IN	20	JTAG to FPGA
ULI_SYSTEM / XIO	IN	4	FPGA access W22 PIN
FPGA_IO	INOUT	10	FPGA access U22 PIN (PUDC)
RESIN	IN	16	RESETIN from B2B connector (Negative Reset)
DONE	IN	28	FPGA Configuration DONE_0 Pin
PROG_B	OUT	27	FPGA Configuration PROGRAM_B_0 Pin
PGOOD	OUT	12	PGOOD to B2B connector
3.3V / PG_SENSE	IN	25	from module generated 3.3V Voltage
EN1	IN	11	Power Enable from B2B Connector (Positive Enable)
SYSLED2 / LED1	OUT	8	Module LED D2 (Red)
SYSLED1/ LED2	OUT	9	Module LED D1 (Green)

Name / opt. VHD Name	Direction	Pin	Description
MODE		13	/ currently_not_used
NOSEQ		14	/ currently_not_used
ULI_CPLD		5	/ currently_not_used

2.2 Functional Description

2.2.1 JTAG

JTAG signals routed directly through the CPLD to FPGA. Access between CPLD and FPGA can be multiplexed via JTAGEN (logical one for CPLD, logical zero for FPGA).

2.2.2 Power

PGOOD is zero, if EN1 or PG_SENSE is zero else high impedance state.

PUDC is high during FPGA power up.

2.2.3 FPGA Configuration

FPGA configuration process will be stared, if RESIN, PG_SENSE and EN1 is ONE.

2.2.4 LED

LED	STATUS	Condition	User defined
LED1 (Red)	ON	RSIN=0	---
LED1 (Red)	Blink	RSIN=1, DONE=0	---
LED1 (Red)	X	RSIN=1, DONE=1	FPGA_IO Pin
LED2 (Green)	ON	RSIN=0	---

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LED	STATUS	Condition	User defined
LED2 (Green)	Blink	RSIN=1, DONE=0	---
LED2 (Green)	X	RSIN=1, DONE=1	XIO Pin

3 Appx. A: Change History

3.1 Revision Changes

3.2 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
📅 2018-05-15	v.24 🔲 Unbekanntes Makro: 'metadata'	REV01	REV01, REV02	@ John Hartfiel	• document style update • add PUDC status
2017-01-26	v.17	REV01	REV01, REV02	John Hartfiel	• Rev01, Firmware released 2014-07-03
2016-11-04	v.1	---		@ John Hartfiel	• Initial release
	All			@ Mohsen Chamanbaz, John Hartfiel	

4 Appx. B: Legal Notices

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📅 2019-06-07